We claim:

1. An electrically operated memory element, comprising:

a volume of memory material programmable to at least a first resistance state and a second resistance state; and

a conductive sidewall spacer in electrical communication with said memory material, said conductive sidewall spacer including at least a first region having a first resistivity and a second region having a second resistivity greater than said first resistivity.

2. The memory element of claim 1, wherein substantially all of said electrical communication is through at least a portion of an edge of said conductive sidewall spacer.

3. The memory element of claim 2, wherein said second region is adjacent to said edge portion, said first region is remote to said edge portion.

4. The memory element of claim 1, wherein said second region is adjacent to said memory material, said first region remote to said memory material.

5. The memory element of claim 1, wherein said memory material is adjacent to at least a portion of an edge of said conductive spacer.

6. The memory element of claim 5, wherein said second region is adjacent to said edge portion, said first region is remote to said edge portion.

7. The memory element of claim 2, wherein said edge is a top edge of said conductive sidewall spacer.

8. The memory element of claim 5, wherein said edge is a top edge of said conductive sidewall spacer.

9. The memory element of claim 1, wherein said conductive sidewall spacer is formed on a sidewall surface selected from the group consisting of trench, via, mesa, and pillar.

10. The memory element of claim 1, wherein said conductive sidewall spacer is single-layered.

11. The memory element of claim 1, wherein said conductive spacer has a narrowed width adjacent said memory material.

12. The memory element of claim 1, wherein said conductive sidewall spacer includes at least one columnar portion protruding toward said memory material.

13. The memory element of claim 1, wherein said memory material is a phase change material.

14. An electrically operated memory element, comprising:

a volume of memory material programmable to at least a first resistance state and a second resistance state; and

a conductive liner in electrical communication with said memory material, said conductive liner including at least a first region having a first resistivity and a second region having a second resistivity greater than said first resistivity.

15. The memory element of claim 14, wherein substantially all of said electrical communication is through at least a portion of an edge of said conductive liner.

16. The memory element of claim 15, wherein said second region is adjacent to said edge portion, said first region is remote to said edge portion.

17. The memory element of claim 14, wherein said second region is adjacent to said memory material, said first region remote to said memory material.

18. The memory element of claim 14, wherein said memory material is adjacent to at least a portion of an edge of said conductive liner.

19. The memory element of claim 18, wherein said second region is adjacent to said edge portion, said first region is remote to said edge portion.

20. The memory element of claim 15, wherein said edge is a top edge of said conductive liner.

21. The memory element of claim 18, wherein said edge is a top edge of said conductive liner.

22. The memory element of claim 14, wherein said conductive sidewall spacer is formed in a via or a trench.

23. The memory element of claim 14, wherein said conductive liner is single-layered.

24. The memory element of claim 14, wherein said conductive liner is cup-shaped having an open-end adjacent said memory material.

25. The memory element of claim 14, wherein said conductive liner includes at least one columnar portion protruding toward said memory material.

26. The memory element of claim 14, wherein said memory material is a phase change material.

27. An electrically operated memory element, comprising:

a volume of memory material programmable to at least a first resistance state and a second resistance state; and

a contact layer in electrical communication with said memory material, substantially all of said electrical communication occurring through at least a portion of an edge of said contact layer, said contact layer including at least a first region having a first resistivity and a second region having a second resistivity greater than said first resistivity.

28. The memory element of claim 27, wherein said second region is adjacent to said edge portion, said first region remote to said edge portion.

29. The memory element of claim 27, wherein second region is adjacent to said memory material, said first region is remote to said memory material.

30. The memory element of claim 27, wherein said contact layer is substantially vertically disposed.

31. The memory element of claim 27, wherein said contact layer is substantially perpendicular to said memory material.

32. The memory element of claim 27, wherein said contact layer is a sidewall layer.

33. The memory element of claim 27, wherein said memory material is a phase change material.

34. An electrically operated memory element, comprising:

a volume of memory material programmable to at least a first resistance state and a second resistance state; and

a contact layer in electrical communication with said memory material, said memory material adjacent to at least a portion of an edge of said contact layer and remote to the remainder of said contact layer, said contact layer including at least a first region having a first resistivity and a second region having a second resistivity greater than said first resistivity.

35. The memory element of claim 34, wherein said second region is adjacent to said edge portion, said first region is remote to said memory material.

36. The memory element of claim 34, wherein said second region is adjacent to said memory material, said first region is remote to said memory material.

37. The memory element of claim 34, wherein said contact layer is substantially vertically disposed.

38. The memory element of claim 34, wherein said contact layer is substantially perpendicular to said memory material.

39. The memory element of claim 34, wherein said contact layer comprises a sidewall layer.

40. The memory element of claim 34, wherein said memory material is a phase change material.

41. A method of making an electrically operated memory element, comprising the steps of:

providing a layer of conductive material;

increasing the resistivity of a portion of said layer, said layer portion including at least a portion of an edge of said layer;

depositing a memory material adjacent said edge portion, said memory material programmable to a first resistance state and a

second resistance state.

42. The method of claim 41, wherein said increasing the resistivity step comprising the step of altering the dopant level of said layer portion.

43. The method of claim 41, wherein said increasing the resistivity step comprises the step of implanting ions into said layer portion.

44. The method of claim 41, wherein said increasing the resistivity step comprises the steps of:

removing said layer portion to form a recess in said layer; and

filling said recess with a material having a resistivity greater than the resistivity of said layer portion.

45. The method of claim 41, wherein said memory material is a phase change material.

46. A method of making an electrically operated memory element, said method comprising the steps of:

depositing a conductive sidewall layer onto a sidewall surface;

forming a top edge to said sidewall layer;

increasing the resistivity of a portion of said sidewall layer, said sidewall layer portion including at least a portion of said top edge;

depositing a memory material adjacent said top edge portion, said memory material programmable to at least a first resistance state and a second resistance state.

47. The method of claim 46, wherein said increasing the resistivity step comprises the step of altering the dopant level of said layer portion.

48. The method of claim 46, wherein said increasing the resistivity step comprises the step of implanting ions into said layer portion.

49. The method of claim 46, wherein said increasing the resistivity step comprises the steps of:

removing said sidewall layer portion to form a recess in said sidewall layer; and

filling said recess with a material having a resistivity greater than said sidewall layer portion.

50. The method of claim 49, wherein said removing step comprises an etching step.

51. The method of claim 46, wherein said memory material is a phase change material.

52. A method of making an electrically operated memory element, comprising the steps of:

forming a conductive sidewall spacer or a conductive sidewall liner;

increasing the resistivity of a portion of said spacer or liner, said spacer or liner portion including at least a portion of an edge of said spacer or liner; and

depositing a memory material adjacent said edge portion of said spacer or liner, said memory material programmable to at least a first resistance state and a second resistance state.

53. The method of claim 52, wherein said increasing the resistivity step comprising the step of altering the dopant level of said spacer or liner portion.

54. The method of claim 52, wherein said increasing the resistivity step comprises the step of implanting ions into said spacer or liner portion.

55. The method of claim 52, wherein said increasing the resistivity step comprises the steps of:

removing said layer portion of said spacer or liner to form a recess in said spacer or liner; and

filling said recess with a material having a resistivity greater than the resistivity of said layer portion.

56. The method of claim 55, wherein said removing step comprises an etching step.

57. The method of claim 52, wherein said memory material is a phase change material.

58. The method of claim 52, wherein said edge is a top edge.